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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,846	08/21/2003	Yoshinori Miyaki	T&A-108-02	6152

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,846	MIYAKI ET AL.	
	Examiner	Art Unit	
	Luan Thai	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/978,708.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

This application appears to be a Continuation of U.S. Application No. 09/978,708, filed October 18, 2001.

Claims **31-43** are pending in this application.

Claims **1-30** have been canceled.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim **33** is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification, as originally filed, does not disclose "*said first ends of said first and second conductive leads are respectively disposed along a phantom line, which extends across said semiconductor integrated chip from the left side of said semiconductor integrated chip to the right side thereof, and wherein a length of said phantom line passing across said semiconductor integrated chip is dimensionally equal or less than a total of the distance between said semiconductor integrated chip and said first conductive lead and that between said semiconductor integrated chip said second conductive lead*", as recited in claim 33.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim **33** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **33**, the claimed of "*said first ends of said first and second conductive leads are respectively disposed along a phantom line, which extends across said semiconductor integrated chip from the left side of said semiconductor integrated chip to the right side thereof, and wherein a length of said phantom line passing across said semiconductor integrated chip is dimensionally equal or less than a total of the distance between said semiconductor integrated chip and said first conductive lead and that between said semiconductor integrated chip said second conductive lead*" is not understood by the examiner as how to measure "*the distance between said semiconductor integrated chip and said first conductive lead and that between said semiconductor integrated chip said second conductive lead*" and which point, the "side" of the leads or the "ends" of the leads, is implied for measuring the distances from such point to the semiconductor chip in order to compare with the "*length of said phantom line passing across said semiconductor integrated chip*". Noted that the examiner has found no support for the claimed limitation above (neither in the specification nor in the drawings).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 31-34, 36-37, 39-40 and 43, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al (6,265,762).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 31-32, 34, 36-37, 39-40, Tanaka et al disclose (see specifically figures 1-7 and 16-19, attachment "1") a semiconductor device comprising: a plurality of inner leads (4) extending around a semiconductor chip (10); a thin sheet-shaped insulating member (7) (Col. 5, lines 43+) supporting the semiconductor chip and joined to an end portion of the respective inner leads; a conductive wire (13) for connecting surface electrodes (11) of the semiconductor chip and the inner leads corresponding thereto; a seal portion (14) in which the semiconductor chip (10), the wire (13), and the insulating member (7) are resin-sealed; and outer leads (5) linked the inner leads (4) and exposed from the seal portion (14), wherein Tanaka et al's figures 6 and 16 show an arrangement pitch

of the surface electrodes (11) of the semiconductor chip (10) is ½ as much as or less than a minimum value of a plurality of a tip pitch between the inner leads (4) adjacent to each other, and figures 16-17 and 19 (attachment "1") show a length (a) of a shorter side of a main surface of the chip (10) formed in a quadrilateral shape being less than or equal to twice a distance (c) from a tip of the inner leads (4) arranged at the farthest location from a center line of the semiconductor chip (10) in a plane direction, to the semiconductor chip (10).

Regarding claim 33, Tanaka et al disclose (see specifically figures 1-7 and 16-19) a semiconductor device comprising: an insulating member (7) having an upper surface and a lower surface; a semiconductor integrated chip (10) having a plurality of bonding pads (11); and first, second, third, and fourth conductive leads (3) disposed respectively in the left, right, upper, and lower sides of the semiconductor integrated chip with respect to a plane direction of the semiconductor integrated chip (see figures 1, 6, 7, and 16-19), wherein each of the first to fourth conductive leads (3) includes a first end (4) having a lower surface connected to a front surface of the insulating member and an upper surface capable of being wire-connected (13) to one of the bonding pads (11), wherein the first ends (4) of the first and second conductive leads (3) are respectively disposed along a phantom line, which extends across the semiconductor integrated chip from the left side of the semiconductor integrated chip to the right side thereof, and wherein a length of the phantom line passing across the semiconductor integrated chip is dimensionally equal to or less than a

total of the distance between the semiconductor integrated chip and the first conductive lead (3) and that between the semiconductor integrated chip and the second conductive lead (3), and further the semiconductor device includes a resin (14) covering the first ends (4), the semiconductor integrated chip (10), and the insulating member (7) and exposing other ends (5) opposite to the first ends (4).

Regarding claim 43, Tanaka et al disclose (see specifically figures 1-7 and 16-19) a semiconductor device comprising: a semiconductor chip (10) having a plurality of surface electrodes (11); a conductive wire (13) connected between a thin-plate-shaped substrate (7/8) supporting the semiconductor chip and the surface electrodes of the semiconductor chip; a resin-sealing portion (14) having upper and lower surfaces and four side surfaces linked therebetween, and sealing the semiconductor chip (10), the wire (13), and the thin-plate-shaped substrate (7/8); and a plurality leads each having a first portion (4) connected to the surface electrodes (11) of the semiconductor chip (10) via conductive wires (13), and a second portion (5) exposed from the resin-sealing portion (14), wherein each end of the plurality of leads (3) and the thin-plate-shaped substrate (7/8) are connected via adhesive layer (7), and wherein the second portions (5) of the plurality of leads (3) are respectively exposed along four sides of the lower surface of the resin-sealing portion (14).

7. Claims 31-34, 36, 37, 39, 40, and 43, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 102(e) as being anticipated by Fogal et al (5,177,032).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 31, 32, 34, 36, 37, 39, 40, and 43, Fogal et al disclose (see specifically figures 3 and 5, attachment "2") a semiconductor device comprising: a plurality of inner leads (18) extending around a semiconductor chip (10); a thin sheet-shaped insulating member (24) supporting the chip and joined to an end portion of the respective inner leads (18); a conductive wires (16) for connecting surface electrodes (14) of the chip and inner leads (18) corresponding thereto. Fogal et al further teach that the assembly is encapsulated in a protective plastic casing (Col. 1, lines 35-38, Col. 2, lines 28-33, and Col. 3, lines 17-21). Although Fogal et al does not specifically disclose a plurality of outer leads linked to the inner leads and exposed from the encapsulated portion, this feature is taken to be inherent teaching of that device since a means of a semiconductor chip package is disclosed and it is apparent that a plurality of outer leads, which are linked to the inner leads and exposed from the encapsulated portion, must be present for getting I/O signal and power source for the device to function as intended. Fogal et al's figure 3 (see attachment "2") shows a length (a) of a shorter side of a main surface of the chip (10) formed in a quadrilateral shape being less than or equal to twice a distance

from a tip of the inner leads (18") arranged at the farthest location from a center line of the semiconductor chip (10) in a plane direction, to the semiconductor chip 10, and an arrangement pitch of the surface electrodes (14) of the semiconductor chip (10) being ½ as much as or less than a minimum value of a tip pitch between the inner leads (18/18") adjacent to each other. Fogal et al further disclose the insulating member (24) being a tape substrate comprising a tape base and an adhesive layer formed on one or both surfaces of the tape base (Col. 3, lines 5+) and inner leads being joined to one another by the adhesive layer (Col. 4, lines 66+, Col. 5, lines 1+). Fogal et al's figure 5 shows the semiconductor chip (10) being thicker than a total thickness of the insulating member (42) and the adhesive layer (46), wherein the adhesive layer (46) is provided through the entirety of the surface of an inner lead arrangement side of the insulating member (42).

Regarding claim 33, Fogal et al disclose (see specifically figures 3 and 5 attached) a semiconductor device comprising: an insulating member (24/42) having an upper surface and a lower surface; a semiconductor integrated chip (10) having a plurality of bonding pads (14); and first, second, third, and fourth conductive leads (18/18") disposed respectively in the left, right, upper, and lower sides of the semiconductor integrated chip with respect to a plane direction of the semiconductor integrated chip, wherein each of the first to fourth conductive leads (18/18") includes a first end having a lower surface connected to a front surface of the insulating member and an upper surface capable of being wire-

connected (16) to one of the bonding pads (14), wherein the first ends of the first and second conductive leads (18") are respectively disposed along a phantom line, which extends across the semiconductor integrated chip from the left side of the semiconductor integrated chip to the right side thereof, and wherein a length (a) of the phantom line passing across the semiconductor integrated chip is dimensionally equal to or less than a total of the distance (c) between the semiconductor integrated chip and the first conductive lead (18") and that between the semiconductor integrated chip and the second conductive lead (18"). Fogal et al further teach that the assembly is encapsulated in a protective plastic casing (Col. 1, lines 35-38, Col. 2, lines 28-33, and Col. 3, lines 17-21).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 35, 38 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al (5,177,032 of record) in view of Newman (5,068,708 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 35, 38 and 42, Fogal et al disclose all the limitations of the claimed invention as detailed above except for the insulating member being a

glass containing epoxy substrate, which contains alumina particles (e.g., ceramic substrate).

Newman while related to a similar chip on tape design teach an insulating member being a glass containing epoxy substrate which contains alumina particles (e.g., ceramic substrate) (Col. 3, lines 23+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use glass-containing epoxy with alumina particles to form the insulating member in Fogal et al device, since such material is commonly used to make an insulating supported member in semiconductor art, as taught by Newman, and such applying is held to be within the ordinary designing ability expected of a person skilled in the art.

5. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al (5,177,032 of record) in view of Templeton et al (5,457,340 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 41, Fogal et al disclose all the limitations of the claimed invention as detailed above except for the adhesive layer being disposed only at an inner lead jointing portion on the surface of the insulating member.

Templeton et al while related to a similar semiconductor structure design discloses (see specifically figure 1) the adhesive layer (105) being disposed only at an inner lead jointing portion on the surface of the insulating member for bonding the inner lead to the insulating substrate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply

Templeton et al's teachings to Fogal et al's device package by forming the adhesive layer only at the lead-joining portion on the surface of the insulating member in order to reduce the adhesive and the manufacturing cost.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2829
September 3, 2004